

You are provided with a schematic of an 8088 “break-out” board which makes the 8088 act much like a microcontroller. This is an embedded application with the purpose of providing a certain number external “ports” (devices) access to the 8088 one byte at a time.

Examine the schematic and answer the below questions. The other chips on the schematic are:

8284 Timer chip
74LS245 Bi-directional, tri-state transceiver
74LS273 Latch (similar to a ‘373)
2764 EPROM chip
6264 Static RAM chip
74LS139 Demultiplexor
74LS240 Uni-directional buffer
74LS241 Uni-directional buffer

Questions:

1. What is the memory capacity of the 2764 EPROM?
2. What is the memory capacity of the 6264 Static RAM?
3. What is the physical memory range of the EPROM chip? (e.g. 0000h-8FFFh)?
4. What is the physical memory range of the RAM chip?
5. The I/O ports are attached through a connector called J1 (see schematic). How many ports can be accessed?
6. Can any of the I/O ports have the same “physical memory” space as the onboard RAM chip? (e.g. are these “isolated I/O” ports accessed via the IO/~M pin?)
7. What is the clock frequency of operation of the 8088?
8. What is the total memory bus cycle period? Recall – there are 4 MPU clock periods per bus period.
9. Are wait states possible in this design? Why or why not?
10. Latency analysis (see chip latencies on next page):
 - a. Say that the 8088 places the address for a data READ from RAM on the bus as expected, during the first half of bus cycle period T1, with a $T_{CLAV}=150\text{ns}$. If the data setup time is $T_{DVCL}=50\text{ns}$, what is the maximum memory latency allowed for the RAM device? Note that this timing is often called “address-to-data-valid”, or t_{AA} in the spec sheets. HINT: You must include propagation delays (latencies) through logic devices!
 - b. The 6264 RAM chip has a maximum latency ($t_{AA}=70\text{ns}$). How fast of an oscillator can you place in the design before WAIT states are required by this chip? Assume the same T_{CLAV} and T_{DVCL} as before. Don’t worry about the other chips like the EPROM or the I/O devices attached externally – you would do the same analysis for those.

Maximum latencies:

74LS139	40ns
74LS240	30ns
74LS32	20ns