8254 Programmable Interval Timer

• Consists of 3 internal, independent programmable timers (16 bits each).
• Each can count in binary or BCD.
• Can be programmed to produce one-shots, act as a square wave generator, a rate generator, etc.
• Can be memory mapped or tied as an isolated I/O device.
• CPU interface – read/write to 8254’s internal registers to configure mode of operation, load initial values, read current values, etc.

8254 pinout & structure

• CS: Enables the 8254
• CLK: Timing source for each of the 3 timers, e.g. pulses applied to CLK0 are used to decrement counter 0.
• G: Gate = 1, enables the counter.
• OUT: Timer waveform output (a clock or a pulse)
• RD: Causes data to be read from the 8254 (IORC)
• WR: Causes data to be written to 8254 (IOWC)

<table>
<thead>
<tr>
<th>A1</th>
<th>A0</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Counter 0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Counter 1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Counter 2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Control</td>
</tr>
</tbody>
</table>
Programming the 8254

- You have to program each timer and give it an initial starting point via the control word.

For example: Send the 8254 CR=10010000 (with A1,A0=11):

- Selects: Counter 2
- Read/Load LS byte only
- Mode 0
- Binary

Example - 1

- Write code to set up three counters located at I/O address 40h as follows:
  - Counter 0: Binary counter operating in mode 0 with a value of 1234h
  - Counter 1: BCD counter operating in mode 2 with a value of 0100h
  - Counter 2: Binary counter operating in mode 4 with a value of 1FFFh

Example - 1, cont’d

Mode word for counter 0 = 00 11 000 0 = 30h
Mode word for counter 1 = 01 11 010 1 = 75h
Mode word for counter 2 = 10 11 100 0 = B8h

Example - 2

- Say we want to read the contents of counter 2 on the fly. The count is to be loaded into the AX register. Assume that the 8254 is located at I/O address 40h
Example – 2, cont’d

• First, latch the contents of counter 2, and then its value can be read from a temporary storage register.

    MOV AL,10000000b ;Latch counter 2
    OUT 43h,AL
    IN 42h,AL ;Read the lower byte
    MOV BL,AL ;Store it temporarily
    IN 42h
    MOV AH,AL
    MOV AL,BL ;Counter contents now resides in AX

8254 Modes of Operation

• MODE 0: Events counter
  – Output becomes logic 0 when control word is written and remains there until N plus the number of programmed counts.
  – Nice for generating termination interrupts

8254 Modes of Operation

• MODE 1: One-shot
  – G triggers the counter.
  – A pulse appears on OUT pin that remains logic 0 for the duration of the count.

8254 Modes of Operation

• MODE 2: Programmable clock generator
  – Produces a pulse, one clock width wide, that is spaced based on the count.
  – Continues until G goes low or a new mode is programmed in.
8254 Modes of Operation

• MODE 3: Square wave generator
  – Generates a continuous square-wave at OUT as long as G is high.
  – If count is EVEN, OUT is hi for ½ the count, low for the other ½.
  – If count is ODD, the output is high for one extra clock period.

8254 Modes of Operation

• MODE 4: Singe-pulse generator (SW one-shot)
  – Produces a single pulse, one clock width wide, that is delayed based on the count.
  – Starts when count is loaded (SW trigger)

8254 Modes of Operation

• MODE 5: Hardware-triggered one-shot
  – Same as mode 4 except that the count is started by a triggered pulse on the G pin instead of by software.

Recall example 1…

• Counter 0: Binary counter operating in mode 0 with a value of 1234h
  – Counter triggered by control word write
  – Output goes high after 1234h (4660d) clock cycles
• Counter 1: BCD counter operating in mode 2 with a value of 0100h
  – Counter triggered by control word write
  – Output pulses low (for one clock cycle) every 0100h (translated to BCD is 4 decimal, see lecture 2, slide 4) clock cycles
• Counter 2: Binary counter operating in mode 4 with a value of 1FFFh
  – Counter triggered by control word write
  – One shot produced after a delay of 1FFFh (=8191d) cycles